

IN THE CLAIMS:

Please add new claims 30-34 and amend the remaining claims as follows:

1. (Previously Presented) An integrated circuit structure comprising:
 - a substrate;
 - first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;
 - second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors;
 - first silicide regions proximate said first spacers of said first-type transistors; and
 - second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.
2. (Previously Presented) The integrated circuit structure in claim 1, wherein said second spacers are only on said etch stop layer on said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

3. (Cancelled).
4. (Original) The integrated circuit structure in claim 1, further comprising:
 - first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors; and
 - second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors.
5. (Original) The integrated circuit structure in claim 4, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.
6. (Original) The integrated circuit structure in claim 4, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.
7. (Original) The integrated circuit structure in claim 1, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).
8. (Previously Presented) An integrated circuit structure comprising:
 - a substrate;

first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;

second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors;

first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors;

second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors;

first silicide regions proximate said first spacers of said first-type transistors; and

second silicide regions proximate said second spacers of said second-type transistors, wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.

9. (Previously Presented) The integrated circuit structure in claim 8, wherein said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors.

10-11. (Cancelled).

12. (Previously Presented) The integrated circuit structure in claim 8, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

13. (Previously Presented) The integrated circuit structure in claim 8, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

14. (Original) The integrated circuit structure in claim 8, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

15-25. (Cancelled).

26. (Currently Amended) An integrated circuit structure comprising:
a substrate;
first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors;
second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop

layer is not on said first spacers that are adjacent said first gate conductors, and wherein said second spacers are only proximate said first spacers that are adjacent said second gate conductors and said second spacers are not proximate said first spacers that are adjacent said first gate conductors;

an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer;

first-type impurity implants in areas of said substrate completely outside of said first spacers of said first gate conductors;

second-type impurity implants in areas of said substrate completely outside of said second spacers of said second gate conductors;

first silicide regions proximate said first spacers of said first-type transistors; and
second silicide regions proximate said second spacers of said second-type transistors,
wherein said second silicide regions are farther from said second gate conductors than said first silicide regions are from said first gate conductors.

27. (Previously Presented) The integrated circuit structure in claim 26, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

28. (Previously Presented) The integrated circuit structure in claim 26, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

29. (Previously Presented) The integrated circuit structure in claim 26, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

30. (New) The integrated circuit structure in claim 1, further comprising an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer.

31. (New) The integrated circuit structure in claim 8, further comprising an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer.

32. (New) The integrated circuit structure in claim 1, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.

33. (New) The integrated circuit structure in claim 8, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.

34. (New) The integrated circuit structure in claim 26, wherein said first spacers and said second spacers each comprise nitride, and wherein said etch stop layer comprises oxide.